AMENDMENTS TO THE SPECIFICATION

Please amend the specification as shown below.

Please amend the paragraph beginning on page 1, line 6, with the following amended paragraph:

The present invention relates to a phase-locked loop circuit and a delay-locked loop circuit, for example, and relates to a phase-locked loop circuit and a delay-locked loop circuit in a digital television set for generating dot clocks.

Please amend the paragraph beginning on page 6, line 20, with the following amended paragraph:

If the reference clock signal φREF is of a low frequency, for example, the horizontal synchronization signal HSYNC of 12 kHz or so, it becomes difficult to include the capacitor CF1 of the lag-lead filter 103 in a semiconductor chip, so it is preferable to make it an external part.

Please amend the paragraph beginning on page 12, line 15, with the following amended paragraph:

The voltage waveform S1FIL has a blunted rising edge waveform changing exponentially by a time constant of the low-pass filter 104. The voltage ΔV1LPO rising exponentially from [tje] the voltage 0 to the voltage ΔV1FIL can be approximated by the following equation:

Please amend the paragraph beginning on page 15, line 19, with the following amended paragraph:

The same reference numerals in FIG. 11 and FIG. [3] 13 indicate the same constituent elements. In addition, the PLL circuit shown in FIG. 13 includes a bias circuit [7] 107, a capacitor CPB, and a capacitor CNB.

Please amend the paragraph beginning on page 33, line 2, with the following amended paragraph:

The phase-locked loop circuit of [,] the present invention may also have a phase comparison means for detecting a size of a leading phase or a delayed phase of a feedback signal with respect to a reference signal and outputting a leading phase signal having a pulse width corresponding to the size of the leading phase or a delayed phase signal having a pulse width correesponding to the size of the delayed phase, a smoothing means for smoothing the leading phase signal or the delayed phase signal output from the phase compairson means and outputting the result as a control signal, a bias signal generating means for outputting a first bias signal and a second signal corresponding to the control signal, a nose filter for removing noise components included in the first bias signal and the second signal, a first superposing means for superposing the leading phase signal or the delayed phase signal output from the phase comparison means on the first bias signal, a second superposing means for superposing the leading phase signal or the delayed phase signal output from the phase comparison means on the seocnd bias signal, and an oscillation cirucit which includes a plurality of delay stages for exchanging and outputting a first current variable according to the first bias signal superposed with other signals by the first superposing means and a second current variable according to the second bias signal superposed with other signals by the second superposing

means according to levels of input signals, feeds back an output signal of a last delay stage to an input of a first delay stage, and outputs an output signal of one of the delay stages as the feedback signal to the phase comparison means.

Please amend the paragraph beginning on page 45, line 20, with the following amended paragraph:

The PLL circuit of the present invention shown in FIG. 1 differs from the PLL circuit of the prior art shown in FIG. [9] 11 in the points that in the PLL circuit in FIG. 1, the capacitor CU and capacitor CD are provided on the output line of the low-pass filter 4, the outputs of the phase comparator 1, that is, the up signal UP and down signal /DOWN, are input to these capacitors, and a rectangular pulse waveform is input to the voltage-controlled oscillator accoridng to the voltage-division ratio of the capacitances of the capacitor CLP of the low-pass filter and these capacitors.

Please amend the paragraph beginning on page 47, line 15, with the following amended paragraph:

In addition, the down signal DOWN, for example, is input to the gate of [a] an n-channel MOS transistor on a not shown ground line side of the charge pump circuit. By inputting a high level pulse signal to the down signal DOWN, the n-channel MOS transistor is turned on, and the charging and discharging current ICP is supplied to the lag-lead filter 3.

Please amend the paragraph beginning on page 52, line 19, with the followning amended paragraph:

Waveform diagram of FIG. [4 Fshows] 4F shows the waveform of the bias voltage PBIAS.

Please amend the paragraph beginning on page 59, line 10, with the following amended paragraph:

The points of difference of the sixth embodiment of the present invention shown in FIG. 8 and the fifth embodiment of the present invention shown in FIG. 7 lie in the fact that in the present embodiment shown in FIG. 7, a pulse control circuit [8] 2 is provided between the phase comparator 1 and the charge pump circuits and the magnitude of the output current ICP2 of the charge pump 22 is variable according to the current selection signals SELICPn-1 to SELICP0 and in the fact that a low-pass filter 4 is provided between the lag-lead filter 3 and the bias circuit 7 and ab ias signal can be obtained from the output of the low-pass filter 4.

Please amend the paragraph beginning on page 62, line 17, with the following amended paragraph:

The pulse control circuit [8] 2 receives the up signal UP and the down signal DOWN of the phase comparator 1 and supplies the up signal /Upn and the down signal DOWNn to the charge pump circuit 21.